That Which Is Claimed Is:

1. A method of bumping a substrate including a metal layer thereon, the method comprising:

forming a barrier layer on the substrate including the metal layer;

forming a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is offset from the metal layer; and

after forming the conductive bump, removing at least some of the barrier layer from the metal layer thereby exposing the metal layer while maintaining a portion of the barrier layer between the conductive bump and the substrate.

2. A method according to Claim 1 wherein the substrate comprises an integrated circuit substrate.

3. A method according to Claim 1 wherein the metal layer comprises an aluminum layer.

4. A method according to Claim 1 wherein the barrier layer comprises a layer of TiW.

5. A method according to Claim 1 wherein the metal layer, the barrier layer, and the conductive bump all comprise different materials.

6. A method according to Claim 1 further comprising:

before forming the conductive bump, forming a conductive under bump metallurgy layer on the barrier layer; and

before removing the barrier layer, removing the conductive under bump metallurgy layer from the barrier layer opposite the metal layer while maintaining a portion of the conductive under bump metallurgy layer between the conductive bump and the substrate.

7. A method according to Claim 6 wherein the conductive under bump metallurgy layer comprises copper.

8. A method according to Claim 6 wherein the conductive under bump metallurgy layer and the barrier layer comprise different materials.

9. A method according to Claim 6 further comprising:

before forming the conductive bump, forming a second barrier layer on the under bump metallurgy layer wherein the second barrier layer and the under bump metallurgy layer comprise different materials and wherein the second barrier layer is between the conductive bump and the conductive under bump metallurgy layer.

10. A method according to Claim 9 wherein the second barrier layer comprises nickel.

11. A method according to Claim 10 wherein the under bump metallurgy layer comprises copper.

12. A method according to Claim 9 wherein forming the second barrier layer comprises selectively forming the second barrier layer on a portion of the under bump metallurgy layer wherein the second barrier layer is offset from the metal layer.

13. A method according to Claim 12 wherein forming the conductive bump comprises selectively forming the conductive bump on the second barrier layer offset from the metal layer.

14. A method according to Claim 13 wherein selectively forming the second barrier layer and selectively forming the conductive bump comprise

selectively forming the second barrier layer and the conductive bump using a same mask.

15. A method according to Claim 1 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

16. A method according to Claim 1 wherein forming the conductive bump comprises selectively plating the bump on the barrier layer offset from the metal layer.

17. A method according to Claim 1 wherein the integrated circuit substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein the conductive bump is formed on the barrier layer opposite the input/output pad.

18. A method according to Claim 17 wherein the metal layer and the bump pad both comprise aluminum.

19. A method according to Claim 1 wherein the substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein after removing the barrier layer from the metal layer, the conductive bump is electrically coupled to the input/output pad.

20. A method according to Claim 19 wherein the metal layer and the input/output pad both comprise aluminum.

21. A method according to Claim 19 wherein the conductive bump is formed on the barrier layer opposite the input/output pad.

22. A method according to Claim 19 wherein the conductive bump is offset from the input/output pad.

23. A method according to Claim 1 further comprising:

after removing the barrier layer from the metal layer, bonding a second substrate to the conductive bump.

24. An electronic device comprising:

a substrate including an exposed metal layer thereon;

a barrier layer on the substrate offset from the exposed metal layer; and

a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the conductive bump is offset from the metal layer, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

25. An electronic device according to Claim 24 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

26. An electronic device according to Claim 24 wherein the barrier layer comprises titanium tungsten.

27. An electronic device according to Claim 25 wherein the exposed metal layer comprises aluminum.

28. An electronic device according to Claim 25 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

29. An electronic device according to Claim 24 further comprising a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

30. An electronic device according to Claim 24 further comprising:

a second substrate bonded to the conductive bump.

31. An electronic device according to Claim 24 further comprising an input/output pad on the integrated circuit substrate wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

32. An electronic device according to Claim 31 wherein the input/output pad and the metal layer each comprise aluminum.

33. An electronic device according to Claim 31 wherein the conductive bump is on the barrier layer opposite the input/output pad.

34. An electronic device according to Claim 31 wherein the conductive bump is offset from the input/output pad.

35. An electronic device according to Claim 25 further comprising:

an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.

36. A method of bumping an electronic device comprising a substrate including an exposed metal layer thereon, the method comprising

forming a barrier layer on the substrate offset from the exposed metal layer; and

forming a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the

conductive bump is offset from the metal layer, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

37. A method according to Claim 36 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

38. A method according to Claim 36 wherein the barrier layer comprises titanium tungsten.

39. A method according to Claim 38 wherein the exposed metal layer comprises aluminum.

40. A method according to Claim 38 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

41. A method according to Claim 36 further comprising:

forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

42. A method according to Claim 36 further comprising:

bonding a second substrate bonded to the conductive bump.

43. A method according to Claim 36 wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

44. A method according to Claim 43 wherein the input/output pad and the metal layer each comprise aluminum.

45. A method according to Claim 43 wherein the conductive bump is on the barrier layer opposite the input/output pad.

46. A method according to Claim 43 wherein the conductive bump is offset from the input/output pad.

47. A method according to Claim 36 further comprising:

an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.

48. A method of bumping an integrated circuit substrate including a metal layer thereon, the method comprising:

forming a barrier layer on a substrate including the metal layer;

forming a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is laterally offset from the metal layer; and

after forming the conductive bump, removing the barrier layer from the metal layer thereby exposing the metal layer while maintaining a portion of the barrier layer between the conductive bump and the substrate.

49. An integrated circuit device comprising:

an integrated circuit substrate;

an exposed metal layer on the integrated circuit substrate;

a barrier layer on the integrated circuit substrate laterally offset from the exposed metal layer; and

a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is remote from the metal layer.